REMARKS

In an Office Action mailed on March 8, 2006, claims 20-28, 35, 37 and 39-47 were allowed; claims 48 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Faulcon in view of Sharma; and claims 49-51 were objected to as being dependent upon a rejected base claim but were indicated as being allowable if rewritten in independent form. Newly-added claims 52-56 are patentable for at least the reason that the cited prior art fails to teach or suggest a regulator to regulate a timing relationship between a data bit signal and a strobe signal based on the degree of skew that is indicated by a duty cycle, for the reasons that are discussed below in connection with claim 48. Claim 25 has been amended to correct a clerical error.

Regarding the § 103 rejection of claim 48, the Examiner contends that Faulcon is silent whether the output signal of the phase detector 14 is a pulse train signal whose duty cycle increases if the skew increases and decreases if the skew decreases. Office Action, 3. However, Applicant submits that Faulcon is explicit that the output signal that is generated by the phase detector 14 does not indicate a degree of skew.

More specifically, Faulcon states in paragraph 36 that the phase information 28 includes a late/early signal 52, "which indicates whether delayed data signal 26 is early or late with respect to delayed clock signal 22." Furthermore, in paragraph 36, Faulcon states that the phase information 28 includes the "enable signal 50, which indicates when the late/early signal is valid." As set forth in paragraph 37, an up/down counter 58 of the phase accumulator 16 counts up when the late/early signal is valid and late and counts down when the late/early signal 52 is early and valid.

Thus, the signal that is provided by the Faulcon's phase detector 14 merely indicates whether the data signal is behind or ahead of the clock signal. The early/late signal does not, however, constitute a signal whose duty cycle indicates a degree of skew between the data and clock signals. Thus, for example, if the data signal is early with respect to the clock signal, the early/late signal would maintain the same logical state, regardless of how early the data signal is (i.e., to the clock signal). Likewise, if the data signal is late with respect to the clock signal, the early/late signal would maintain the opposite logical state, regardless of how late the data signal

is respect to the clock signal. Thus, the early/late signal fails to indicate a degree of skew, whether via a duty cycle or any other characteristic of the late/early signal.

Therefore, Faulcon also fails to disclose regulating a timing relationship between a data bit signal and a strobe signal based on a degree of skew that is indicated by a duty cycle, as the phase accumulator 16 merely increases or decreases the selectable delay 18 based on whether the data signal is late with respect to the clock signal. However, there is no teaching or suggestion in Faulcon regarding regulating a timing relationship between the data and clock signals based on a degree of skew indicated by a duty cycle. Therefore, even assuming, for purposes of argument, that a suggestion or motivation exists for the combination of Faulcon and Sharma, this combination fails to teach or suggest all claim limitations, such as the act of regulating the timing relationship based on a degree of skew indicated by a duty cycle. For at least this reason, Applicant submits that a *prima facie* case of obviousness has not been set forth for independent claim 48 and requests withdrawal of the § 103 rejection of this claim.

CONCLUSION

In view of the foregoing, Applicant respectfully requests a favorable action in the form of a Notice of Allowance. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504 (ITL.0294US).

Respectfully submitted,

Date: June 8, 2006

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